**IN THE CLAIMS**:

Please amend the claims as follows:

1-16. (Canceled)

17. (Currently Amended) A signal transmission system comprising:

a write amplifier;

a sense amplifier connected to the write amplifier via a data bus; and

a semiconductor memory device for writing data from the write amplifier to the sense amplifier, the semiconductor memory device comprising a signal transmission line for transmitting data without requiring precharging for every bit, wherein when writing, at least during a portion of a period when a select signal for connecting said data bus to said sense amplifier is being supplied a bit line connected to said sense amplifier for amplification is disconnected from said sense amplifier, thereby allowing information on said data bus to be transferred at high speed into said sense amplifier,

wherein said signal transmission line comprises a plurality of switchable signal transmission lines organized in a branching structure or a hierarchical structure, at least one target unit from which to read data is connected to each of said plurality of switchable signal transmission lines;

a readout circuit for eliminating an intersymbol interference component is connected to said signal transmission line; and

an intersymbol interference component elimination circuit for reducing noise introduced when said signal transmission line is switched between said plurality of switchable signal transmission lines, and thereby provides a smooth intersymbol

precharged to a predetermined voltage level before switching to said second signal transmission line.

24. (Previously Presented) A semiconductor memory device as claimed in claim 20, wherein said readout circuit employs a partial-response detection method, and said readout circuit employing said partial-response detection method corrects the intersymbol interference component elimination function when said signal transmission line is switched, by varying an input capacitance value.

25. (Original) A semiconductor memory device as claimed in claim 24, wherein said readout circuit employing said partial-response detection method includes: an intersymbol interference estimation means for estimating intersymbol interference from a previously received signal; and a decision means for making a logic decision on a currently received signal by subtracting said estimated intersymbol interference from said currently received signal.

26. (Previously Presented) A semiconductor memory device as claimed in claim 24, wherein said readout circuit employing said partial-response detection method includes first and second partial-response detection amplifiers arranged in parallel with each other, and wherein said first partial-response detection amplifier performs an intersymbol interference estimation operation while said second partial-response detection amplifier is performing a data decision operation and, at the next timing, said first partial-response detection amplifier performs the data decision operation while said second partial-response detection amplifier is performing the intersymbol interference estimation operation.

36. (Previously Presented) A semiconductor memory device as claimed in claim 20, wherein from said sense amplifier the data is first transferred onto a local data bus via a selected column gate, and then onto a global data bus via a local data bus switch that selects said local data bus, and said data is amplified by a complementary-type data bus amplifier having the intersymbol interference component elimination function, thereby continuing data transmission uninterruptedly without performing data bus precharge during data transfer.

37. (Currently Amended) A semiconductor memory device as claimed in claim 20, wherein a read-select pulse width of a read select signal for selecting the connection between said at least one target unit and a data bus for data read is made shorter than a write-select pulse width of a write select signal for selecting the connection between said at least one target unit and said data bus for data write.

38. (Previously Presented) A semiconductor memory device as claimed in claim 20, wherein during a continuous cycle period, whether read or write cycles, data bus precharge is rendered unnecessary at least for activated buses.

39. (~~Previously Presented~~ Currently Amended) A semiconductor memory device as claimed in claim 20, wherein in any data bus state except for [[a]] continuous read and write cycle periods, a read precharge level is set at a different level than a write precharge level.

40. (Previously Presented) A semiconductor memory device employing a signal transmission system for transmitting data without requiring precharging comprising:

a signal transmission line for transmitting data without requiring precharging for every bit, said signal transmission line comprises a plurality of switchable transmission

function, thereby continuing data transmission uninterruptedly without performing data bus precharge during data transfer.

45. (Currently Amended) A semiconductor memory device as claimed in claim 40, wherein a read-select pulse width of a read select signal for selecting a connection between said target unit and [[said]] a data bus for data read is made shorter than a write-select pulse width of a write select signal for selecting the connection between said target unit and said data bus for data write.

46. (Previously Presented) A semiconductor memory device as claimed in claim 40, wherein during a continuous cycle period, whether read or write cycles, data bus precharge is rendered unnecessary at least for activated buses.

47. (Previously Presented) A semiconductor memory device as claimed in claim 40, wherein in any data bus state except for continuous read and write cycle periods, a read precharge level is set at a different level than a write precharge level.

48. (Canceled)

49. (Currently Amended) A semiconductor memory device comprising:

a plurality of blocks; and

a state latch circuit for holding at least two states consisting of a CURRENT state indicating [[the]] a bus currently in an active state and a NEXT state indicating [[the]] a bus to be selected and activated next, or four states consisting of said CURRENT state, said NEXT state, a STANDBY state indicating [[the]] a bus in a standby state, and a PREVIOUS state indicating [[the]] a bus just deactivated,

plurality of

wherein each of said blocks cycles through the four states, changing state from the STANDBY state to the NEXT state to the CURRENT state to the PREVIOUS state and then back to the STANDBY state.

50. (Currently Amended) A semiconductor memory device comprising:

a plurality of blocks; and

a state latch circuit for holding at least two states consisting of a CURRENT state indicating [[the]] a bus currently in an active state and a NEXT state indicating [[the]] a bus to be selected and activated next, or four states consisting of said CURRENT state, said NEXT state, a STANDBY state indicating [[the]] a bus in a standby state, and a PREVIOUS state indicating [[the]] a bus just deactivated,

wherein when [[one]] a block of said plurality of blocks is in the STANDBY state, a signal input for raising a word line within said block is enabled; when said block is in the NEXT state, said block is in a state ready to read data from a unit target or a sense amplifier onto a bus or ready to write data to the unit target or the sense amplifier, with said word line rising and said sense amplifier activated at least at the end of said NEXT state ~~period~~; when said block is in the CURRENT state, data is being read out of or being written in said block; and when said block is in the PREVIOUS state, data is rewritten, and then said word line is lowered and a bit line is precharged.

51. (Currently Amended) A semiconductor memory device comprising:

a plurality of blocks; and

a state latch circuit for holding at least two states consisting of a CURRENT state indicating [[the]] a bus currently in an active state and a NEXT state indicating [[the]] a bus to be selected and activated next, or four states consisting of said CURRENT state,

the row blocks that are activated at the same time during said period, data on said global data bus transferred from said local data bus are continuously read out.

57. (Currently Amended) A semiconductor memory device as claimed in claim 56, further comprising:

a memory cell [[or]] and a sense amplifier for reading data in said memory cell transfers data onto said local data bus by a row selection line and a column select signal, wherein the local data bus is selected in accordance with a row block select signal, and at least one local data bus is connected to said global data bus; and

a complementary-type partial response detection bus amplifier connected to said global data bus, wherein an intersymbol interference component on said global data bus is eliminated, thereby providing high-speed data read.

58. (Currently Amended) A semiconductor memory device as claimed in claim 56, including a holding circuit which, after switching is made from a first local data bus to a second local data bus, holds [[the]] a selected state of ~~the~~ a row selection line in the row block having said first local data bus for a prescribed amount of time, thus enabling the local data bus switching between a plurality of activated row blocks.

59. (Currently Amended) A semiconductor memory device as claimed in claim 58, further including a decoder and a row selection line holding circuit which latches a row address into said decoder in accordance with a row address latch signal given to each row block, selects a designated row selection line within said each row block, and holds said row selection line in its selected state for ~~a~~ the prescribed amount of time or until a signal for initializing said decoder is input.

60. (Previously Presented) A semiconductor memory device as claimed in claim 59, wherein said decoder and said row selection line holding circuit share address lines with other decoders and other row selection line holding circuits provided for other row blocks, latch ~~said~~ an address signal and select the designated row selection line in the block for which the row address latch signal given to each of said row blocks is valid, and prevent row selection lines from transitioning in other blocks for which said row address latch signal is not valid.

61. (Currently Amended) A semiconductor memory device as claimed in claim 59, wherein said decoder and said row selection line holding circuit comprise a dynamic logic circuit and a switch means for controlling the activation of said dynamic logic circuit, and when said row address is input at an input of said dynamic logic circuit, and said switch means is on, transition of a data decoder output section is enabled, and when said switch means is off, transition of said data decoder output section is prohibited to hold the state of said row selection line.

62. (Previously Presented) A semiconductor memory device as claimed in claim 61, wherein said decoder and said row selection line holding circuit hold the state of said row selection line for a finite amount of time.

63. (Previously Presented) A semiconductor memory device as claimed in claim 59, wherein said decoder and said row selection line holding circuit include the holding circuit, provided for each row block, for holding the address to be input to said decoder for each row block, and hold the state of said row selection line by holding said address for each row block.

when writing, at least during a portion of a period when a select signal for connecting said data bus to said sense amplifier is being supplied, a bit line connected to said sense amplifier for amplification is disconnected from said sense amplifier, thereby allowing information on said data bus to be transferred at high speed into said sense amplifier,

wherein after activating a selected row block, said data bus is precharged before writing data to a first sense amplifier and after writing data is done to a final sense amplifier.

74. (Previously Presented) A semiconductor memory device comprising:

a write amplifier; and

a sense amplifier coupled to the write amplifier via a data bus, wherein data is written from the write amplifier to the sense amplifier, and

when writing, at least during a portion of a period when a select signal for connecting said data bus to said sense amplifier is being supplied, a bit line connected to said sense amplifier for amplification is disconnected from said sense amplifier, thereby allowing information on said data bus to be transferred at high speed into said sense amplifier,

wherein the data bus precharges before supplying said select signal is rendered unnecessary at least during a period when a plurality of continuous write cycles are being performed.

75. (Previously Presented) A semiconductor memory device comprising:

a write amplifier; and

a sense amplifier coupled to the write amplifier via a data bus, wherein data is written from the write amplifier to the sense amplifier, and

when writing, at least during a portion of a period when a select signal for connecting said data bus to said sense amplifier is being supplied, a bit line connected to said sense amplifier for amplification is disconnected from said sense amplifier, thereby allowing information on said data bus to be transferred at high speed into said sense amplifier,

said semiconductor memory device further includes a latch-type sense amplifier, and the connection between said sense amplifier and said bit line is controlled by a bit line transfer gate with a control signal applied to said bit line transfer gate and operated quickly for disconnection and slowly for connection.

76. (Original) A semiconductor memory device as claimed in claim 75, wherein the control signal applied to said bit line transfer gate is formed so that said bit line rises slowly or in a steplike manner in order to prevent inversion of data latched in said sense amplifier.

77. (Previously Presented) A semiconductor memory device as claimed in claim 76, wherein the control signal applied to said bit line transfer gate is generated by being delayed through delay means so that said control signal rises slowly, or is generated by a circuit having a plurality of switching transistors whose sources are coupled to different voltages or whose gates are supplied with different control voltages so that said control signal rises in the steplike manner.

78. (Previously Presented) A semiconductor memory device comprising:

a write amplifier; and